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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/735,630	12/14/2000	Hiroaki Ozeki	43890-468	5850

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EXAMINER	
WARE, CICELY Q	
ART UNIT	**PAPER NUMBER**
2634	6

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/735,630	OZEKI ET AL.	
	Examiner	Art Unit	
	Cicely Ware	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7 and 10-14* is/are rejected.

7)☒ Claim(s) *4-6,8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

a. Pg. 3, line 20, applicant uses the phrase "diagram of method". Examiner suggests using "diagram of a method" for clarification purposes.

b. Pg. 3, line 23, applicant uses the phrase "speed when a operation-starting point". Examiner suggests using "speed when an operation-starting point" for clarification purposes.

c. Pg. 6, lines 27, applicant uses the phrase "to of the dynamic ". Examiner suggests using "to the dynamic" for clarification purposes.

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's Admitted cooperation is requested in correcting any errors of which applicant may become aware in the specification. Appropriate correction is required.

Claim Objections

3. Claims 1,7, 6, 10, 11,12, 13 and 14 are objected to because of the following informalities:

a. Applicant uses the phrase "with digitally-modulated" and "by digitally modulated". Examiner suggests applicant re-write this phrase for clarification purposes.

b. Pg. 19, line 16, applicant uses the phrases "shifted with using the control voltages". Examiner suggests using "shifted using the control voltages" for clarification purposes.

c. Pg. 23, examiner suggests applicant move line 26 to the following page.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted prior art (Fig. 13) in view of Kawai (US Patent 6,631,171).

(1) With regard to claim 1, applicant discloses a prior art digital signal receiver (Fig. 13) comprising: an input terminal (101) for receiving an input signal digitally-modulated; at least two variable gain amplifiers (102, 104) coupled in series to said input terminal for controlling the level of the input signal; an analog-to-digital converter (106) for receiving an output of said variable gain amplifier (104); a level comparator (112) coupled to an output of said A/D converter (106) for comparing a level of the output of said A/D converter and a reference level; a loop filter (113) coupled to said level comparator (112); and a control voltage generator (114) for generating control voltages for controlling said variable gain amplifiers based on an output of said loop

filter. However Applicant's Admitted prior art does not disclose wherein an operation-starting point of any of said variable gain amplifiers is shifted using control voltages.

However Kawai discloses in (Fig. 1 (2,3,6,7), Fig. 2, Fig. 3, Fig. 6) wherein an operation-starting point of any of said variable gain amplifiers is shifted using control voltages (col. 1, lines 53-64, col. 4, lines 34-66, col. 6, lines 9-12, 17-21).

Therefore it would have been obvious to one of ordinary skill in the art to modify Applicant's Admitted prior art to incorporate wherein an operation-starting point of any of said variable gain amplifiers is shifted using control voltages as a known method of controlling the level of the modulated signal which differs when the gain is changed or attenuation is started in the variable gain amplifier (Kawai col. 1, lines 45-51).

(2) With regard to claim 2, claim 2 inherits all the limitations of claim 1. Kawai further discloses wherein the operation-starting point is shifted when the operation-starting point is the same as a level of the input signal (col. 1, lines 37-44).

(3) With regard to claim 3, claim 3 inherits all the limitations of claim 1. Kawai further discloses wherein the operation-starting point is shifted when a level of the input signal is at a saturation point of said any of said variable gain amplifiers (col. 2, lines 3-36).

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted prior art (Fig. 13) in view of Abbott et al. (US Patent 5,375,145).

With regard to claim 7, Applicant's Admitted prior art discloses a digital signal

receiver (Fig. 13) comprising: an input terminal (101) for receiving an input signal digitally-modulated; at least two variable gain amplifiers (102, 104) coupled in series to said input terminal for controlling the level of the input signal; an analog-to-digital converter (106) for receiving an output of said variable gain amplifier (104); a level comparator (112) coupled to an output of said A/D converter (106) for comparing a level of the output of said A/D converter and a reference level; a loop filter (113) coupled to said level comparator (112); and a control voltage generator (114) for generating control voltages for controlling said variable gain amplifiers based from an output of said loop filter. However Applicant's Admitted prior art does not disclose wherein a bandwidth of said loop filter is controlled with using the control voltages.

However Abbott et al. discloses a digital gain control loop wherein a bandwidth of the loop filter is controlled by using the control voltages (col. 13, lines 27-39).

Therefore it would have been obvious to one of ordinary skill in the art modify Applicant's Admitted prior art to disclose a loop filter where the bandwidth is controlled by using the control voltages in order to provide greater loop stability and immunity to noise artifacts (Abbott et al. col. 13, line 25).

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted prior art (Fig. 13) in view of Genossar et al. (US Patent 6,643,321).

With regard to claim 10, applicant discloses in (Fig. 13) a prior art digital signal receiver comprising: an input terminal (101) for receiving an input signal with digitally modulated, a variable gain amplifier (102, 104) coupled to said input terminal for

controlling a level of the input signal, an analog-to-digital converter (106) for receiving an output of said variable gain amplifier, a demodulator (107) for demodulating an output of said A/D converter, a ghost detector coupled to an output of said demodulator for detecting a delay time of ghost. However Applicant's Admitted prior art does not disclose the ghost detector comprising: a delay unit for delaying the output of said demodulator, a ghost calculator for calculating the delay time and an energy of ghost, a coefficient unit, and an averaging unit for calculating a coefficient of said coefficient unit.

However Genossar et al. discloses in (Fig. 2(54, 24), Fig. 3A) an adaptive equalizer comprising: a delay unit for delaying the output of said demodulator, an LMS unit for calculating the delay time and an energy of ghost, a coefficient unit, and an averaging unit for calculating a coefficient of said coefficient unit, wherein a number of times of averaging at said averaging unit is controlled based on the delay time (col. 1, lines 56-60, 64-67, col. 2, line 1, col. 11, lines 7-26, col. 12, lines 19-33, col. 13, lines 1-4).

Genossar et al. does not explicitly disclose an averaging unit and an LMS unit. However it is well known in the art that an LMS algorithm is an adaptive algorithm for averaging to obtain tap coefficients and energy is always transferred when there is a delay in time.

Therefore it would have been obvious to one of ordinary skill in the art to modify Applicant's Admitted prior art to disclose wherein the ghost detector/ equalizer comprises a delay unit for delaying the output of said demodulator, a ghost calculator/LMS unit for calculating the delay time and an energy of ghost, a coefficient

unit, and an averaging unit for calculating a coefficient of said coefficient unit; wherein a number of times of averaging at said averaging unit is controlled based on the delay time to process the digital signal in order to compensate for interference which occurs when two or more symbols of the transmission signal interfere with each other.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted prior art (Fig. 13) in view of Kasuga et al. (US Patent 4,355,304).

With regard to claim 11, applicant discloses in (Fig. 13) a prior art digital signal receiver comprising: an input terminal (101) for receiving an input signal digitally-modulated, a variable gain amplifier (102, 104) coupled to said input terminal for controlling a level of the input signal, an analog-to-digital converter (106) for receiving an output of said variable gain amplifier, a level comparator (112) coupled to an output of said A/D converter (106) for comparing a level of the output of said A/D converter and a reference level; a loop filter (113) coupled to said level comparator (112); a demodulator (107) for demodulating an output of said A/D converter, a ghost detector/equalizer(107) coupled to an output of said demodulator for detecting a delay time of ghost. However Applicant's Admitted prior art does not disclose wherein an operation-starting point of said variable gain amplifier is shifted based on the delay time.

However Kasuga et al. discloses a digital compandor wherein an operation-starting point of said variable gain amplifier is shifted based on the delay time (Fig. 2, col. 4, lines 51-67, col. 5,lines 1-5).

Therefore it would have been obvious to one of ordinary skill in the art to modify Applicant's Admitted prior art to disclose wherein an operation-starting point of the variable gain amplifier is shifted based on the delay time to maintain a signal capacity in a predetermined range to enhance transmission quality (Kasuga et al. col. 2, lines 3-9).

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted prior art (Fig. 13) in view of Abbott et al. (US Patent 5,375,145).

With regard to claim 12, applicant discloses in (Fig. 13) a prior art digital signal receiver comprising: an input terminal (101) for receiving an input signal digitally-modulated, a variable gain amplifier (102, 104) coupled to said input terminal for controlling a level of the input signal, an analog-to-digital converter (106) for receiving an output of said variable gain amplifier, a level comparator (112) coupled to an output of said A/D converter (106) for comparing a level of the output of said A/D converter and a reference level; a loop filter (113) coupled to said level comparator (112); a demodulator (107) for demodulating an output of said A/D converter, a ghost detector/equalizer(107) coupled to an output of said demodulator for detecting a delay time of ghost. However Applicant's Admitted prior art does not disclose wherein a bandwidth of said loop filter is controlled based on the delay time.

However Abbott et al. discloses a digital loop filter wherein a bandwidth of the loop filter is controlled based on the delay time (col. 13, lines 27-39).

Therefore it would have been obvious to one of ordinary skill in the art to modify Applicant's Admitted prior at to disclose wherein a bandwidth of the loop filter is

controlled based on the delay time because a narrow level loop bandwidth provides for greater loop stability and immunity to noise artifacts (Abbott et al. col. 13, lines 24-25).

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted prior art (Fig. 13) in view of Takaki (US Patent 6,032,031).

With regard to claim 13, applicant discloses in (Fig. 13) a prior art digital signal receiver comprising: an input terminal (101) for receiving an input signal digitally-modulated, a variable gain amplifier (102, 104) coupled to said input terminal for controlling a level of the input signal, an analog-to-digital converter (106) for receiving an output of said variable gain amplifier, a level comparator (112) coupled to an output of said A/D converter (106) for comparing a level of the output of said A/D converter and a reference level; a loop filter (113) coupled to said level comparator (112). However Applicant's Admitted prior art does not disclose a carrier-to-noise ratio detector coupled to the output of said A/D converter for detecting a carrier-to-noise ratio of an input signal into said A/D converter, wherein an operation-starting point of said variable gain amplifier is shifted based on the CN ratio.

However Takaki discloses a receiver comprising an error ratio detector coupled to the output of said A/D converter for detecting an error ratio of an input signal into the A/D converter, wherein an operation-starting point of the variable gain amplifier is shifted based on the CN ratio (abstract, col. 5, lines 32-61, col. 6,lines 43-50, col. 8, lines 36-65, col. 11, lines 19-29).

Therefore it would have been obvious to one of ordinary skill in the art to modify Applicant's Admitted prior art to disclose a carrier-to-noise ratio detector coupled to the output of the A/D converter for detecting a carrier-to-noise ratio of an input signal into the A/D converter, wherein an operation-starting point of the variable gain amplifier is shifted based on the CN ratio in order to suppress distortion components produced by non-linearity of high-frequency amplifier (Takaki col. 4, lines 12-15).

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted prior art (Fig. 13) in combination with Takaki (US Patent 6,032,031) as applied to claim 13 above, and further in view of Abbott (US Patent 5,375,145).

With regard to claim 14, claim 14 inherits all the limitations of claim 13. However Applicant's Admitted prior art in combination with Takaki do not disclose wherein a bandwidth of said loop filter is controlled based on the CN ratio.

However Abbott et al. discloses a digital loop filter wherein the bandwidth of the loop filter is controlled based on the CN ratio (col. 13, lines 12-39).

Therefore it would have been obvious to one of ordinary skill in the art to modify the inventions of Applicant's Admitted prior art in combination with Takaki to disclose wherein the bandwidth of the loop filter is controlled based on the CN ratio in order to provide greater loop stability and immunity to noise artifacts.

Allowable Subject Matter

12. Claims 4, 5, 6, 8, 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. The prior art made record of and not relied upon is considered pertinent to Applicant's Admitted disclosure.

a. Otani et al. US Patent 5,452,332 discloses an AGC Circuit for Burst Signal.

b. Rakib et al. US Patent 6,665,308 discloses an apparatus and method for equalization in distributed digital data transmission systems.

c. Debus, Jr., et al. US Patent 4,550,415 discloses a fractionally spaced adaptive equalizer.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cicely Ware whose telephone number is 703-305-8326. The examiner can normally be reached on Monday – Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Cicely Ware

cqw
February 5, 2004

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